

AMENDMENTS TO THE SPECIFICATION

Please amend the Title of the Invention as follows:

~~METHOD FOR FORMING MRAM BIT MEMORY CELL HAVING [[A]] AN
ELECTROPLATED BOTTOM SENSE LAYER UTILIZING ELECTROLESS PLATING~~

Replace the paragraph inserted on page 1, before "Field of the Invention" by the first preliminary amendment dated January 22, 2004, with the following, which contains updated information:

This application is a divisional of application Serial No. 10/146,890 filed May 17, 2002, now U.S. Pat. No. 6,716,644.

Amend paragraph [0007] on page 3 as follows:

FIG. 2 illustrates a side sectional view of the MRAM stacks 22 of FIG. 1. As shown, pinned layer 20 and sense layer 21 are comprised of several individual layers, including a bottom conductive barrier layer 24 formed of, for example, Ta, at the base of the pinned layer 20. The barrier layer ~~20~~ 24 also lines the trenches in which the bit lines 18 are formed. Also, pinned layer 20 and sense layer 21 are separated by a magnetically and electrically nonconductive tunnel junction layer 25, for example, Al_2O_3 .

Amend paragraph [0034] on page 8 as follows:

Although FIG. 5 schematically-illustrates mask 56 positioned over the photoresist layer 55, those skilled in the art will appreciate that mask 56 is typically spaced from the photoresist layer 55 and light passing through mask 56 is ~~foecussed~~ focused onto the photoresist layer 55. After exposure and development of the exposed portions 55a, portions 55b of the unexposed and undeveloped photoresist are left over the insulating layer 54, as shown in FIG. 6. This way, openings 57 (FIG. 6) are formed in the photoresist layer 55.

Amend paragraph [0038] on page 10 as follows:

material layer 60 and ~~protions~~ portions of the barrier layer 59 that are outside of the trenches 58 are removed by means of chemical mechanical polishing (CMP). The top surfaces of the remaining barrier layer 59 inside the trenches 58 and the metal lines 62 are generally flat and uniform across the entire surface of the substrate, as shown in FIG. 11. Each metal line 62 will form the bit or digit line of a conventional MRAM structure.

Amend paragraph [0040] on page 11 as follows:

Referring now to FIG. 12, a first nickel-iron (NiFe) permalloy is provided in the cell shaped openings to form the sense layer 64. The permalloy is electroplated in [[a]] an electroless plating bath for a predetermined period of time depending on the desired thickness. A seed layer is not required as the NiFe is electroplated directly on the first conductor 62 as well and extends to the side walls of the dielectric layer 63. In an

exemplary embodiment of the present invention, the NiFe is electroplated at about 80-90° C. Sense layer 64 and dielectric layer 63 constitute a first magnetic member 79 formed over the first conductor 62. Next, top portions of the sense layer 64 and dielectric layer 63 are pre-sputtered to remove and clean any unwanted portions and to provide a smooth flat surface for the subsequent MRAM cell layers, as described below. Alternatively, chemical mechanical polishing can also be utilized.